



STW13NK100Z

N-channel 1000V - 0.56Ω - 13A - TO-247
Zener - Protected SuperMESH™ PowerMOSFET

General features

| Type | V _{DSS} (@T _{jmax}) | R _{DS(on)} | I _D | P _W |
|-------------|---|---------------------|----------------|----------------|
| STW13NK100Z | 1000 V | < 0.70 Ω | 13 A | 350W |

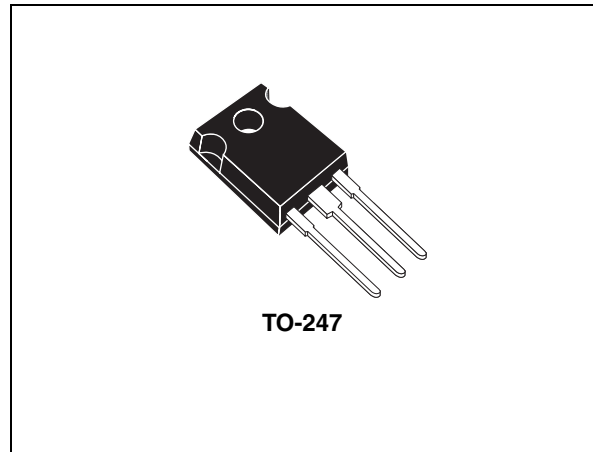
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Description

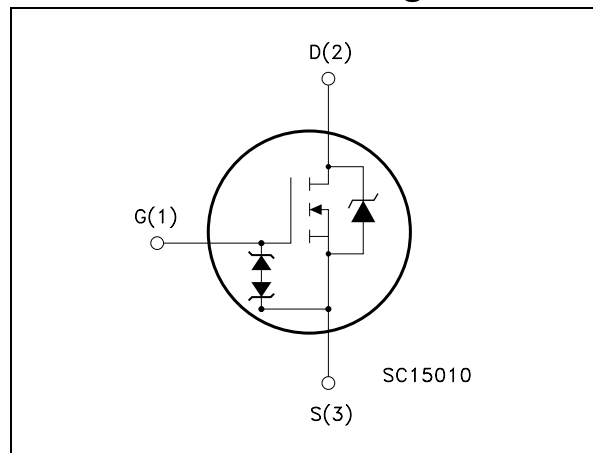
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application



Internal schematic diagram



Order codes

| Part number | Marking | Package | Packaging |
|-------------|-----------|---------|-----------|
| STW13NK100Z | W13NK100Z | TO-247 | Tube |

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1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------------|---|------------|---------------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 1000 | V |
| V_{DGR} | Drain-gate voltage ($R_{GS} = 20K\Omega$) | 1000 | V |
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25^\circ C$ | 13 | A |
| I_D | Drain current (continuous) at $T_C = 100^\circ C$ | 8.2 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 52 | A |
| P_{TOT} | Total dissipation at $T_C = 25^\circ C$ | 350 | W |
| | Derating Factor | 2.7 | W/ $^\circ C$ |
| $V_{ESD (G-S)}$ | Gate source ESD(HBM-C=100pF, R=1,5K Ω) | 6000 | V |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 4 | V/ns |
| T_J | Operating junction temperature | -55 to 150 | $^\circ C$ |
| T_{stg} | Storage temperature | | |

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 8.3 A$, $di/dt \leq 200 A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|--|-------|--------------|
| $R_{thj-case}$ | Thermal resistance junction-case Max | 0.36 | $^\circ C/W$ |
| R_{thj-a} | Thermal resistance junction-ambient Max | 50 | $^\circ C/W$ |
| T_l | Maximum lead temperature for soldering purpose | 300 | $^\circ C$ |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_J Max) | 13 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25^\circ C$, $I_d = I_{AR}$, $V_{dd} = 50V$) | 700 | mJ |

Table 4. Gate-source zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|-------------------------------|--------------------------------------|------|------|------|------|
| BV_{GSO} | Gate-source breakdown voltage | $I_{gs}=\pm 1\text{mA}$ (Open Drain) | 30 | | | V |

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|----------|--------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1mA, V_{GS} = 0$ | 1000 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating},$ $T_c = 125^{\circ}C$ | | | 1 10 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{GS} = 0$) | $V_{GS} = \pm 20V$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 150 \mu A$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10V, I_D = 6.5 A$ | | 0.56 | 0.70 | Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------|---|------|------|------|------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DS} = 15V, I_D = 6.5 A$ | | 14 | | S |
| C_{iss} | Input capacitance | $V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$ | | 6000 | | pF |
| C_{oss} | Output capacitance | | | 455 | | pF |
| C_{rss} | Reverse transfer capacitance | | | 100 | | pF |
| $C_{osseq}^{(2)}$ | Equivalent output capacitance | $V_{GS} = 0, V_{DS} = 0V \text{ to } 800V$ | | 227 | | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 500V, I_D = 7A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 16) | | 45 | | ns |
| t_r | Rise time | | | 35 | | ns |
| $t_{d(off)}$ | Off-voltage rise time | | | 145 | | ns |
| t_f | Fall time | | | 45 | | ns |
| Q_g | Total gate charge | $V_{DD} = 800V, I_D = 13A$ $V_{GS} = 10V$ | | 190 | 266 | nC |
| Q_{gs} | Gate-source charge | | | 30 | | nC |
| Q_{gd} | Gate-drain charge | | | 100 | | nC |

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. $C_{oss eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|-----------------------------------|--|---|-----|--------------------|-----|--------------------|
| I_{SD} | Source-drain current | | | | 13 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 52 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD}=8.3A, V_{GS}=0$ | | | 1.6 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD}=13 A,$ $di/dt = 100A/\mu s,$ $V_{DD}=100 V, T_j=25^\circ C$ (see Figure 18) | | 820 12.7 31 | | ns μC A |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD}=13 A,$ $di/dt = 100A/\mu s,$ $V_{DD}=100V, T_j=150^\circ C$ (see Figure 18) | | 1050 17.8 34 | | ns μC A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

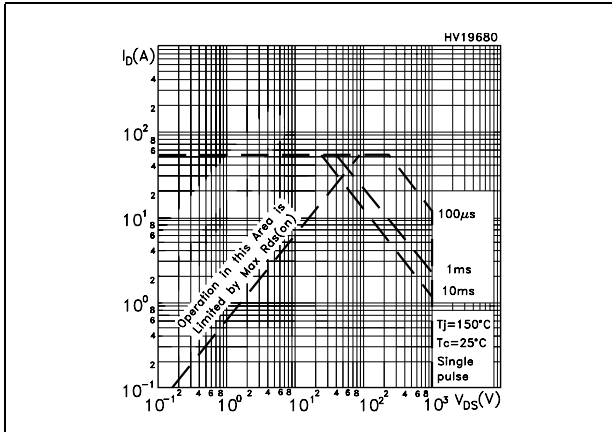


Figure 2. Thermal impedance

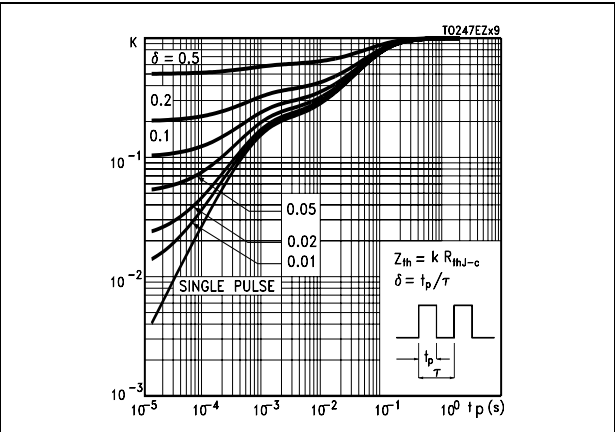


Figure 3. Output characteristics

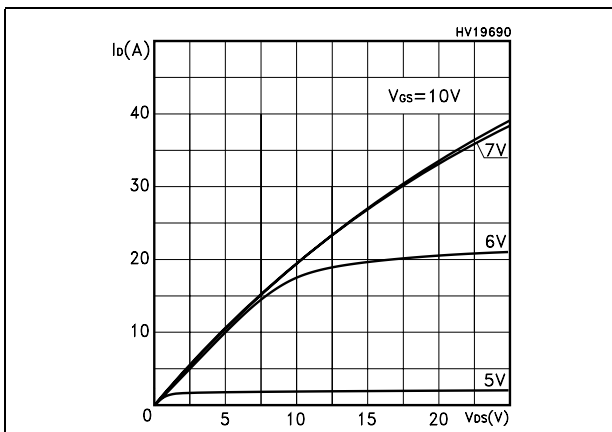


Figure 4. Transfer characteristics

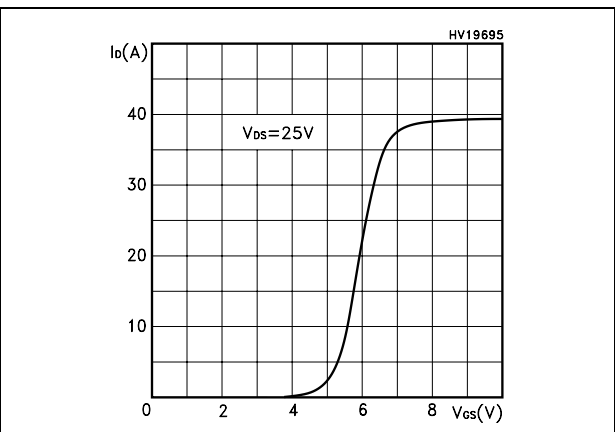


Figure 5. Transconductance

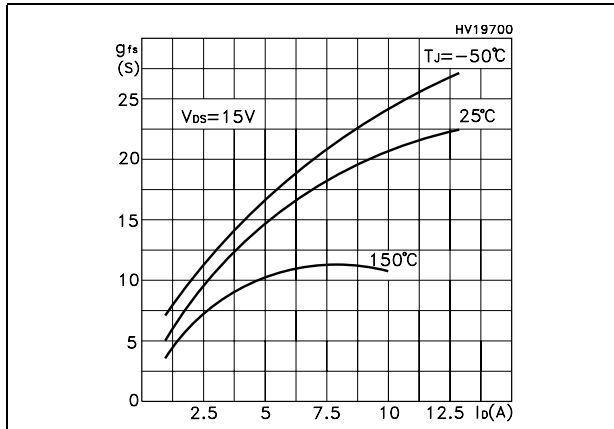


Figure 6. Static drain-source on resistance

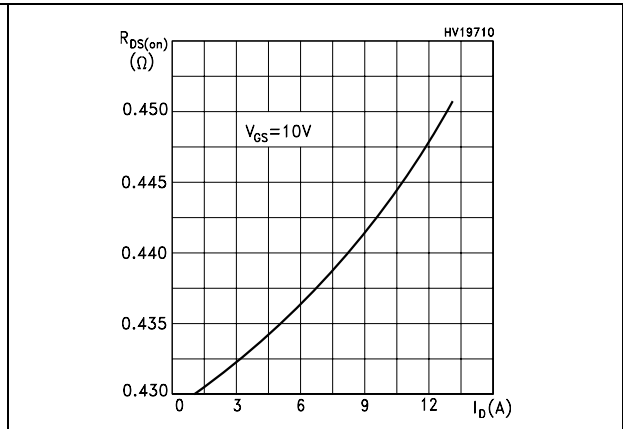


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

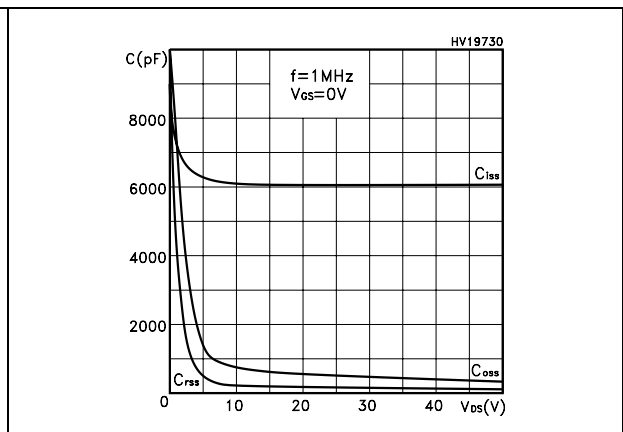
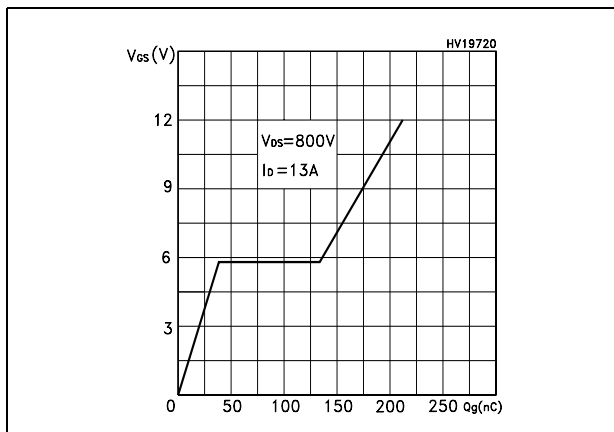


Figure 9. Normalized gate threshold voltage vs temperature

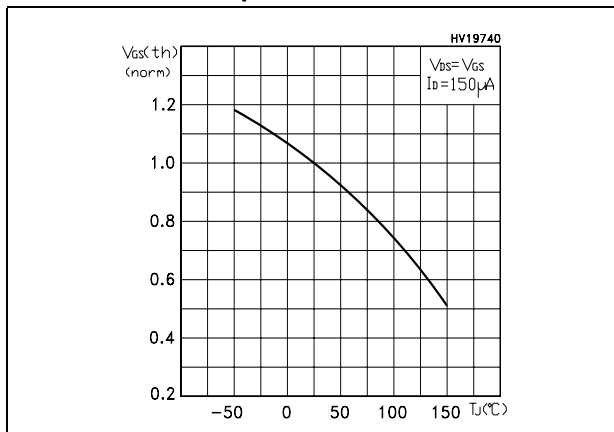


Figure 10. Normalized on resistance vs temperature

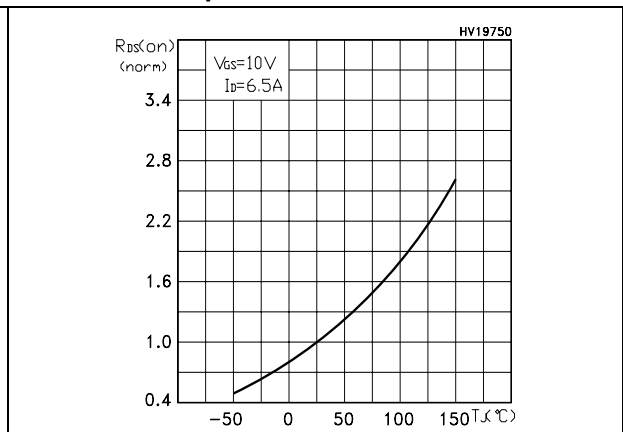


Figure 11. Source-drain diode forward characteristics

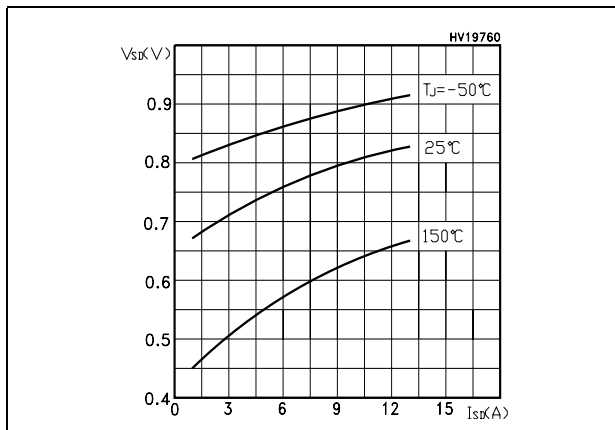


Figure 12. Normalized B_{VDSS} vs temperature

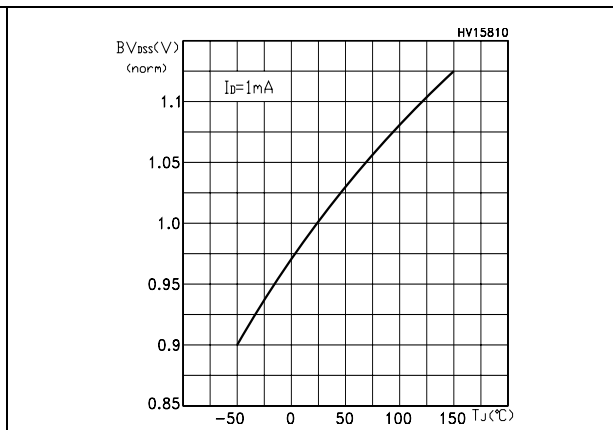
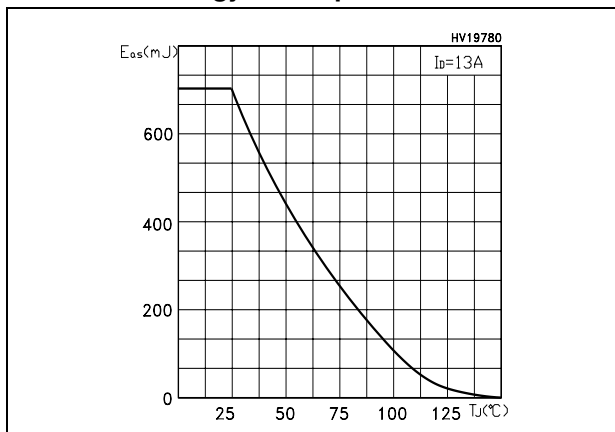


Figure 13. Maximum avalanche energy vs temperature



3 Test circuit

Figure 14. Unclamped Inductive load test circuit

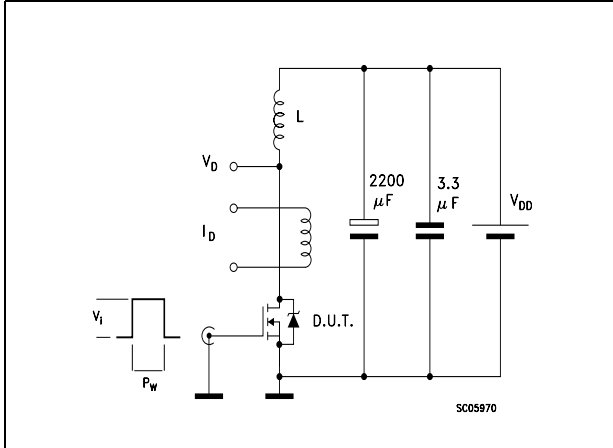


Figure 15. Unclamped Inductive waveform

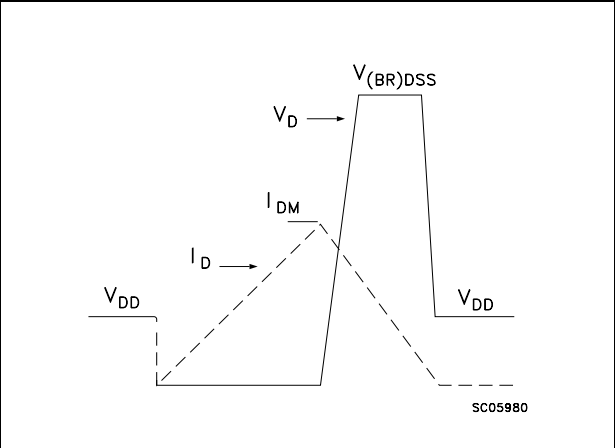


Figure 16. Switching times test circuit for resistive load

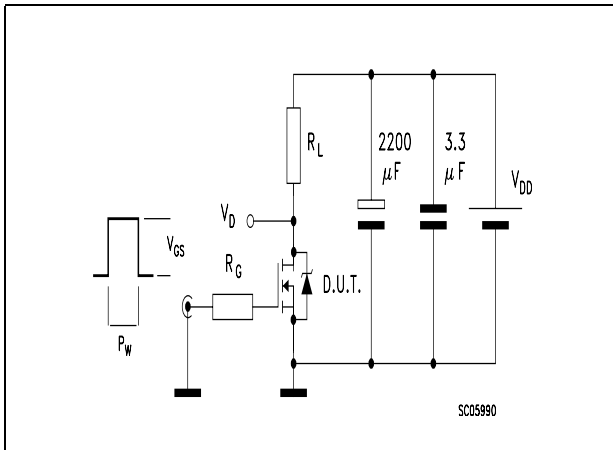


Figure 17. Gate charge test circuit

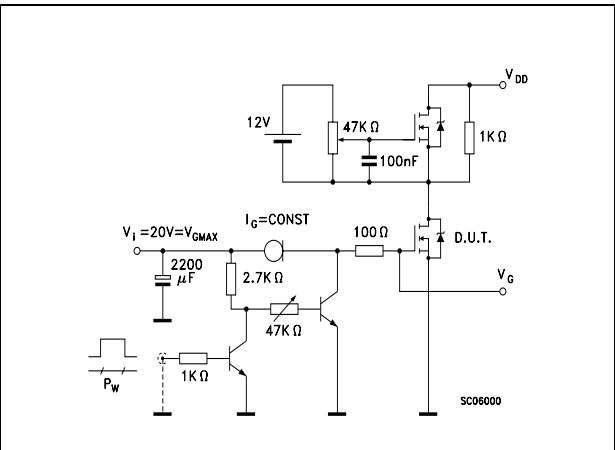
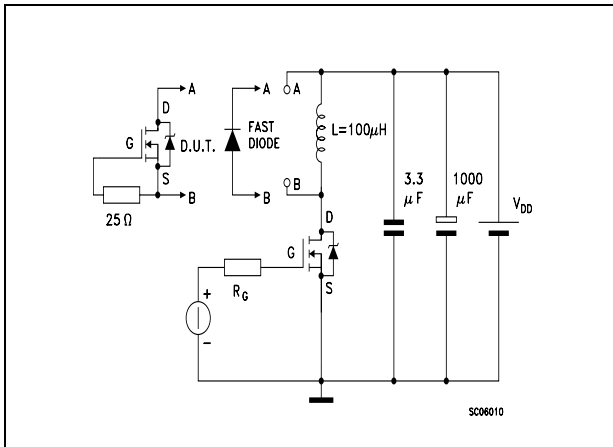


Figure 18. Test circuit for inductive load switching and diode recovery times

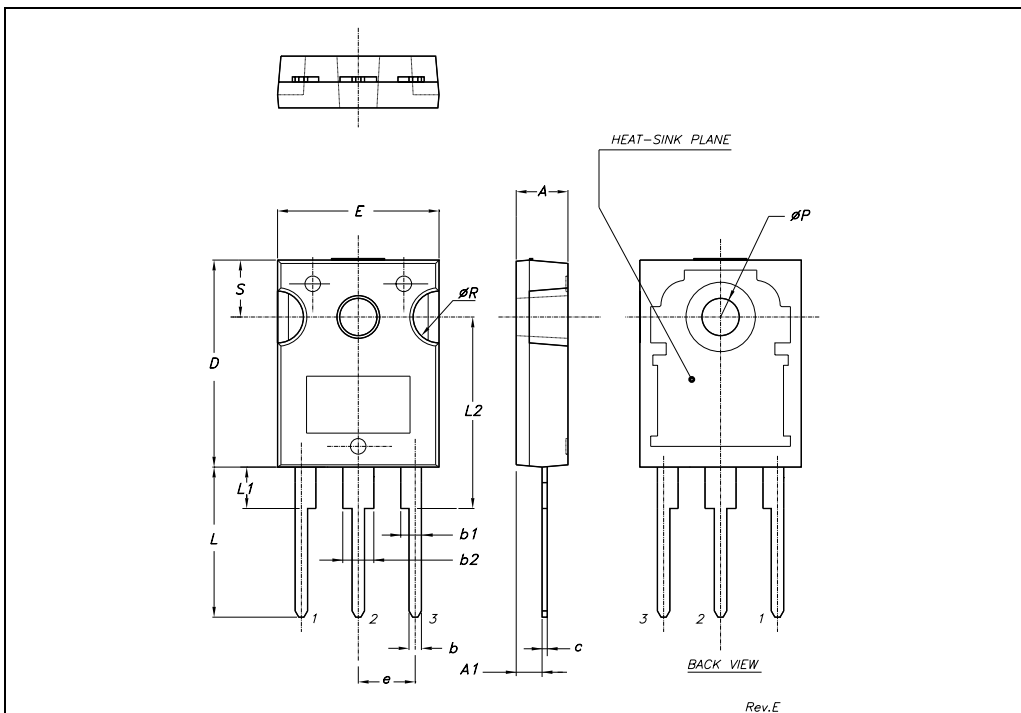


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|-------|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.85 | | 5.15 | 0.19 | | 0.20 |
| A1 | 2.20 | | 2.60 | 0.086 | | 0.102 |
| b | 1.0 | | 1.40 | 0.039 | | 0.055 |
| b1 | 2.0 | | 2.40 | 0.079 | | 0.094 |
| b2 | 3.0 | | 3.40 | 0.118 | | 0.134 |
| c | 0.40 | | 0.80 | 0.015 | | 0.03 |
| D | 19.85 | | 20.15 | 0.781 | | 0.793 |
| E | 15.45 | | 15.75 | 0.608 | | 0.620 |
| e | | 5.45 | | | 0.214 | |
| L | 14.20 | | 14.80 | 0.560 | | 0.582 |
| L1 | 3.70 | | 4.30 | 0.14 | | 0.17 |
| L2 | | 18.50 | | | 0.728 | |
| øP | 3.55 | | 3.65 | 0.140 | | 0.143 |
| øR | 4.50 | | 5.50 | 0.177 | | 0.216 |
| S | | 5.50 | | | 0.216 | |



5 Revision history

Table 8. Revision history

| Date | Revision | Changes |
|-------------|----------|---------------------------------|
| 22-Jun-2004 | 1 | Target document |
| 09-Sep-2004 | 2 | Preliminary document |
| 28-Jan-2005 | 3 | Complete version with curves |
| 18-Sep-2005 | 4 | <i>Figure 12</i> changed |
| 01-Aug-2006 | 5 | New template, no content change |

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