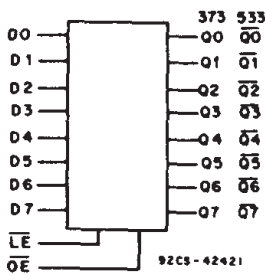


# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533



Data sheet acquired from Harris Semiconductor  
SCHS289



## Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting  
CD54/74AC/ACT533 - Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
4.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$

### FUNCTIONAL DIAGRAM

The RCA-CD54/74AC373 and CD54/74AC533 and the CD54/74ACT373 and CD54/74ACT533 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable ( $\overline{LE}$ ) is HIGH. When the Latch Enable ( $\overline{LE}$ ) goes LOW, the data is latched. The Output Enable ( $\overline{OE}$ ) controls the 3-state outputs. When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT373 and CD54AC/ACT533, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

### TRUTH TABLE

Output Enable	Latch Enable	Data	AC/ACT373 Output	AC/ACT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	I	L	H
L	L	h	H	L
H	X	X	Z	Z

#### Note:

L = Low voltage level  
H = High voltage level  
I = Low voltage level one set-up time prior to the high to low latch enable transition

h = High voltage level one set-up time prior to the high to low latch enable transition.  
X = Don't Care  
Z = High Impedance State

# Technical Data

## CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_i < -0.5$ V or $V_i > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_o < -0.5$ V or $V_o > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_o$ (for $V_o > -0.5$ V or $V_o < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{stg}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

\*For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.

### RECOMMENDED OPERATING CONDITIONS:

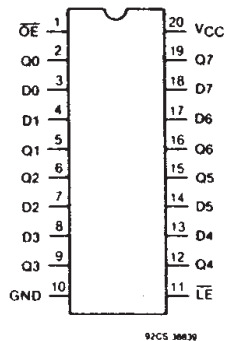
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V
DC Input or Output Voltage, $V_i, V_o$	0	$V_{CC}$	V
Operating Temperature, $T_A$	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

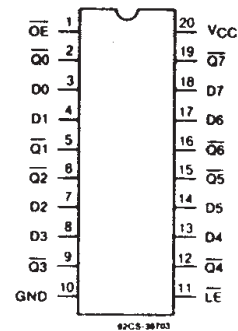
\*Unless otherwise specified, all voltages are referenced to ground.

9

### TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC373, CD54/74ACT373



CD54/74AC533, CD54/74ACT533

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS
				+25		-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	-0.05	1.5	1.4	—	1.4	—	1.4	V
			-0.05	3	2.9	—	2.9	—	2.9	
			-0.05	4.5	4.4	—	4.4	—	4.4	
			-4	3	2.58	—	2.48	—	2.4	
			-24	4.5	3.94	—	3.8	—	3.7	
			-75	5.5	—	—	3.85	—	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	0.05	1.5	—	0.1	—	0.1	—	V
			0.05	3	—	0.1	—	0.1	—	
			0.05	4.5	—	0.1	—	0.1	—	
			12	3	—	0.36	—	0.44	—	
			24	4.5	—	0.36	—	0.44	—	
			75	5.5	—	—	—	1.65	—	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

### ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT373	ACT533
$\overline{OE}$	0.87	0.87
Dn	0.5	0.5
$\overline{LE}$	0.8	0.8

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to LE	t <sub>su</sub>	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to LE	t <sub>h</sub>	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn 373	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	96	—	106	ns
		3.3*	3.1	10.8	3	11.9	
		5†	2.2	7.7	2.1	8.5	
533	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	119	—	131	ns
		3.3	3.8	13.4	3.7	14.7	
		5	2.7	9.5	2.6	10.5	
LE on Qn 373	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.2	4.2	16.8	
		5	3.1	10.9	3	12	
533	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Output Enable Times	t <sub>PZL</sub> t <sub>PZH</sub>	1.5	—	119	—	131	ns
		3.3	4.1	14.4	4	15.8	
		5	2.7	9.5	2.6	10.5	
Output Disable Times	t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5	—	131	—	144	ns
		3.3	3.7	13.1	3.6	14.4	
		5	3	10.5	2.9	11.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	63 Typ.		63 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.  
P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = input frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

# CD54/74AC373, CD54/74AC533 CD54/74ACT373, CD54/74ACT533

**PREREQUISITE FOR SWITCHING: ACT Series**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
LE Pulse Width	t <sub>w</sub>	5†	3.6	—	4	—	ns
Setup Time Data to LE	t <sub>su</sub>	5	2	—	2	—	ns
Hold Time Data to LE	t <sub>h</sub>	5	2.7	—	3	—	ns

†5 V: min. is @ 4.5 V

**SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn 373	t <sub>PLH</sub>	5†	2.7	9.5	2.6	10.4	ns
	t <sub>PHL</sub>		3	10.4	2.9	11.4	
LE to Qn 373 533	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.1	11.4	3	12.5	ns
Output Enable Times	t <sub>PZL</sub> t <sub>PZH</sub>	5	3.5	12.3	3.4	13.5	ns
Output Disable Times	t <sub>PLZ</sub> t <sub>PHZ</sub>	5	3.2	11.4	3.1	12.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	63 Typ.		63 Typ.		pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per latch.

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC} \text{ where } f_i = \text{input frequency}$$

C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

9



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54AC373F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54ACT373F3A	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CD54ACT533F3A	OBSOLETE	CDIP	J	20		None	Call TI	Call TI
CD74AC373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74AC373M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74AC373M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT373E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74ACT373M	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74ACT373M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.